AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (ORIGINAL) A method of estimating an error in a data recovery system, comprising the steps of:

(A) receiving one or more data pulses each having a data rate;

(B) receiving a plurality of clock signals each having a rate similar to the data rate and having a substantially equal phase offset from each other;

(C) clocking the one or more data pulses with each of the plurality of clock signals to determine a particular offset of each of the one or more data pulses;

(D) counting a number of said one or more data pulses received at different phase offsets;

(E) providing a value representing a ratio of the counts at different clock phase offsets; and

(F) determining said error for the received data pulses in response to the value.

2. (ORIGINAL) The method according to claim 1, wherein step (C) further comprises the sub-steps of:

(C-1) applying the one or more data pulses to each of a plurality of registers, each clocked by a different one of the plurality of clock signals; and

(C-2) determining which of the plurality of registers first clocks each of the one or more data pulses.

3. (ORIGINAL) The method according to claim 2, wherein step (C) further comprises the sub-steps of:

(C-3) incrementing one of a plurality of counters each time a register associated with a particular counter is determined to have first clocked a particular data pulse; and

(C-4) determining the count of at least one counter when at least one other counter reaches a predetermined value.

4. (ORIGINAL) The method according to claim 1, wherein step (F) further comprises:

checking a look-up table for an error rate corresponding to the value.

5. (ORIGINAL) The method according to claim 4, wherein step (D) further comprises the sub-step of:

(D-1) incrementing a first counter when a first one or more of said plurality of clock signals comprises a first predetermined phase offset for a particular data pulse or

incrementing a second counter when a second one or more of said plurality of clock signals comprises a second predetermined phase offset for a particular data pulse.

6. (ORIGINAL) The method according to claim 5, wherein step (D) further comprises the sub-step of:

(D-2) determining when one of the two counters reaches a predetermined value; and

(D-3) determining the count of the other of the two counters; and

(D-4) determining an error rate from a look-up table in response to said count of the other counter.

7. (ORIGINAL) The method according to claim 1, wherein step (D) further comprises the sub-steps of:

(D-1) incrementing a first counter when a first one or more of said plurality of clock signals comprises a first predetermined phase offset for a particular data pulse or incrementing a second counter when a second one or more of said plurality of clock signals comprises a second predetermined phase offset for a particular data pulse;

(D-2) determining when one of the two counters reaches a predetermined value; and

(D-3) determining the count of the other of the two counters; and wherein the count of the other counter is then compared to the predetermined value and used to determine whether a skew error is positive or negative.

8. (ORIGINAL) An apparatus for estimating an error in a data recovery system, comprising:

a circuit configured to receive data pulses at a data rate and a plurality of clock signals each having a rate similar to the data rate and having a substantially equal phase offset from each other;

a data clocking device configured to receive said data pulses and said plurality of clock signals and provide a plurality count signals, when a data pulse is clocked by a clock signal at an associated clock input for counting the number of data pulses received at different phase offsets and to provide a value representing a ratio of the counts at different clock phase offsets; and

a plurality of counters each configured to receive one or more of said count signals, wherein said device is configured to provide an error for the received data pulses based on the counts at different clock phase offsets.

9. (ORIGINAL) The apparatus according to claim 8, wherein the data clocking comprises:

a plurality of registers each configured to receive said data pulse and one or more of said plurality of clock inputs; and

a discriminating device coupled to said plurality of registers, wherein one or more of the plurality of registers is configured to provide a count signal for each data pulse received depending on which register is first to clock the particular data pulse.

10. (ORIGINAL) The apparatus according to claim 9, wherein a first counter has a maximum value and is configured to provide an indication when the maximum value is reached.

11. (ORIGINAL) The apparatus according to claim 10, further comprising:

a second counter configured to provide an indication of the value reached when the first counter reaches the maximum value.

12. (ORIGINAL) The apparatus according to according to claim 11, wherein there are four registers, each receiving one of the four clock signals at the second input thereof.

13. (ORIGINAL) The apparatus according to claim 12, wherein the discriminating device comprises:

one or more logic gates, coupled to one or more registers;

one or more multiplexers each coupled to an output of said one or more registers and one or more of said logic gates; and

a second one or more registers each coupled to an output of said one or more multiplexers.

14. (ORIGINAL) The apparatus according to claim 13, wherein the first OR gate has a first and a second input coupled to the outputs of the two second registers corresponding to the two registers clocked by clock signals having phase offsets of 0° and 90° and the second OR gate has a first and a second input coupled to the outputs of the two second registers corresponding to the two registers clocked by clock signals having phase offsets of 180° and 270°.

15. (ORIGINAL) The apparatus according to claim 14, wherein a first counter is incremented when either one of two registers clocked by clock signals having phase offsets of 0° and 90° first clocks a particular data pulse and a second counter is incremented when either one of two registers clocked by clock

signals having phase offsets of 180° and 270° first clocks a particular data pulse.

16. (ORIGINAL) The apparatus according to claim 15, wherein the device includes a look-up table which provides an error rate for the received data pulses based on the ratio of the values of the two counters.

17. (ORIGINAL) The apparatus according to claim 13, wherein the first OR gate has a first and a second input coupled to the outputs of the two second registers corresponding to the two registers clocked by clock signals having phase offsets of 0° and 270° and the second OR gate has a first and a second input coupled to the outputs of the two second registers corresponding to the two registers clocked by clock signals having phase offsets of 90° and 180°.

18. (ORIGINAL) The apparatus according to claim 17, wherein a first counter is incremented when either one of two registers clocked by clock signals having phase offsets of 0° and 270° first clocks a particular data pulse and a second counter is incremented when either one of two registers clocked by clock signals having phase offsets of 90° and 180° first clocks a particular data pulse.

19. (ORIGINAL) The apparatus according to claim 18, wherein the device includes a comparator to determine which of the two counters has a higher value so as to provide an indication of whether a skew error is positive or negative.